Q.P.Code: 20EC0448	R20	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech II Year II Semester Regular & Supplementary Examinations August-2023

DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Simplify the following Boolean expression: F = (A+B)(A'+C)(B+C).	CO1	L3	6M
	b	Simplify the following Boolean expression: F = XY+XYZ+XYZ'+X'YZ	CO1	L3	6M

OR

2		What is Grey code? What are the rules to construct gray code? Develop the 4 bit gray code for the decimal 0 to 15.	CO1	L1	12M

UNIT-II

3		Simplify the following Boolean expressions using K-map. F(A, B, C, D,E)= Σm(0,2,4,6,9,11,13,15,17,21,25,27,29,31)	CO2	L3	12M

OR

4		What are the universal gates? Implement logic gates by using NAND and NOR gates.	CO2	L3	12M

UNIT-III

5		Design & implement Half Adder and Full Adder with truth table.	CO3	L3	12M

OR

6		Design 32 to1 multiplexer using 8 to 1 multiplexers and 2to4 Decoder.	CO4	L3	12M

UNIT-IV

7	a	Explain working of Master Slave Flip flop with neat diagram.	CO5	L1	6M
	b	Draw the logic diagram T Flip Flop by using JK Flip Flop and draw the timing diagram.	CO5	L1	6M

OR

8		Implement 4-bit ring counter using suitable shift register. Briefly describe its operation.	CO5	L3	12M

UNIT-V

9		Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7).	CO6	L3	12M

OR

10		Compare three combinational circuits: PLA, PAL and PROM.	CO6	L3	12M

***** END *****